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IN THE SPECIFICATION

Please replace the paragraph beginning on page 20, line 22 with the following rewritten paragraph.

E' --The first and second pull-up transistors 32 and 36 of the SRAM memory cells 30 making up each row of the memory array 90 are preferably formed within the same N-well as shown in Fig. 7. Four N-wells 64<sub>1</sub>-64<sub>4</sub> with each of the first and second pull-up transistors 32 and 3634 for each memory cell 30 in each row sharing a respective N-well are shown in Fig. 7. For illustrative purposes, the two horizontal boxes of each cell represent the gate connections for each pull-up transistor 32, 3634 while the vertical box represents the active areas for the transistors 32, 3634. It will be appreciated by those skilled in the art that the first and second pull-down transistors 3436, 38 for each memory cell 30 would be appropriately formed on both sides of the respective N-wells 64<sub>1</sub>-64<sub>4</sub>.--